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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,155	07/30/2003	Yi Ding	M-15222 US	1880

7590 09/29/2005

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EXAMINER	
NHU, DAVID	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/632,155	DING, YI	
	Examiner	Art Unit	
	David Nhu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 June 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-42* is/are pending in the application.

4a) Of the above claim(s) *1-21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *22-42* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *03*. (11-9-04; 6-2-05; 4-20-04)
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Final

DETAILED ACTIONS

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 22-42 are rejected under 35 U.S.C. 102(b) as being anticipated by Ogura et al (6,388,293 B1), and Harari et al (6,420,231 B1).

Regarding claim 22, Ogura, (see figures 1, 35, 14, col. 5, lines 50-67, col. 6, lines 1-67, col. 7, lines 1-53, col. 17, lines 28-67, col. 18, lines 1-21), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 121, 122 of a first conductivity n-type in a semiconductor substrate 10 and having a channel region 110 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 140 comprising a semiconductor material (polysilicon) of a second conductivity p-type opposite to the first conductivity n-type, the first conductive gate overlying a portion of the channel region 110; and forming a floating gate 241 overlying a portion of the channel region (see figure 14, col. 17, lines 28-67, col. 2, lines 35-67).

Regarding claims 23-32, Ogura, (see figures 1-5, col. 6-9, lines 1-67), also teaches the channel region comprises a surface region underlying the first conductive gate and having a lower dopant concentration of the second conductivity type than a region

immediately below the surface region; the surface region is at 0.20 micro meter deep (see col.7, lines 37-43); implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to be below the first conductive gate; wherein the first conductive gate is to turn on the underlying portion of the channel region to provide access to the memory cell; wherein the floating gate is one of two floating gates of the nonvolatile memory cell, each floating gate overlying a portion of the channel region; wherein the first conductivity type is type N; wherein the second conductivity type is type P.

Regarding claim 22, Harari, (see figures 4, 5, col. 8, lines 1-39), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 49, 51 of a first conductivity type in a semiconductor substrate 45 and having a channel region L1-L2 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 55-58 comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and forming a floating gate 55-58 overlying a portion of the channel region. L1-L2.

Regarding claim 23, Harari, (see col. 8, lines 15-18), teaches wherein the first conductive gate is a gate of a buried channel transistor.

Regarding claim 33, Ogura, (see figures 1, 13, 14, col. 17, lines 28-67), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain region having source/drain regions 221, 222 of a first conductivity n-type in a semiconductor substrate 10 and having a channel region 110 in the

semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 140 overlying a portion of the channel region 110; and forming a floating gate 241 overlying a portion of the channel region wherein the first conductive gate is a gate of a buried channel transistor (211) (see figure 14, col. 17, lines 28-67, col. 2, lines 35-67).

Regarding claim 22, Harari, (see figures 4, 5, col. 8, lines 1-39), teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory cell having source/drain regions 49, 51 of a first conductivity type in a semiconductor substrate 45 and having a channel region L1-L2 in the semiconductor substrate between the source/drain regions, the method comprising: forming a first conductive gate 55-58 comprising a semiconductor material of a second conductivity type opposite to the first conductivity type, the first conductive gate overlying a portion of the channel region; and forming a floating gate 55-58 overlying a portion of the channel region., wherein the first conductive gate is a gate of a buried channel transistor.

Regarding claims 34-42, Ogura, (see figures 1-5, col. 6-9, lines 1-67), also teaches the channel region comprises a surface region underlying the first conductive gate and having a lower dopant concentration of the second conductivity type than a region immediately below the surface region; the surface region is at 0.20 micro meter deep (see col.7, lines 37-43); implanting an impurity of the first conductivity type into a surface region of the channel region, wherein the surface region is to be below the first conductive gate; wherein the first conductive gate is to turn on the underlying portion of the channel region to provide access to the memory cell; wherein the floating gate is

one of two floating gates of the nonvolatile memory cell, each floating gate overlying a portion of the channel region; wherein the first conductivity type is type N; wherein the second conductivity type is type P.

Response to Arguments

3. Contrary to the applicant's argument about claims 22, 33 in his remarks, pages 6, Ogura (6,388,293 B1) does not teach the floating gate 140 but it is a electrode gate or a conductive gate. In fact, Ogura also teach a floating gate 241 overlying a portion of the channel region 110 (see figures 14); also in figure 3, the floating gate 141 overlying a portion of the channel region 110.

Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure: Eitan'725, Morii'979, Chang'115, Perlegos'776 are cited as of interest.

5. A shortened statutory period for response to this action is set to expired 3 (three) months from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see 710.02 (b)).

6. Any inquiry concerning this communication on earlier communications from the examiner should be directed to David Nhu, (571)272-1792. The examiner can normally be reached on Monday-Friday from 7:30 AM to 5:00 PM. The examiner's supervisor, David Nelms can be reached on (571)272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703)872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Information regarding the status of an application may be obtained from the patent application information retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

David Nhu

March 24, 2005